

APPENDIX B
VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

CLAIMS:

1. (Twice Amended) A MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising:
 - a P-type substrate having substantially flat, parallel upper and lower surfaces;
 - a plurality of laterally spaced N-type body regions extending from said upper surface into said substrate;
 - at least one respective P-type source region formed in each of said body regions in said upper surface of said substrate and defining a respective channel region in said upper surface in said N-type body region;
 - a gate electrode comprised of p-type polysilicon disposed atop and insulated from said channel region and operable to invert said channel region in response to the application of a suitable gate voltage to said gate electrode said gate being insulated from said channel region by a gate oxide layer comprising silicon dioxide, said gate oxide layer being radiation hardened and less than 1000Å thick; and
 - a source electrode disposed atop said upper surface and connected to said at least one P-type source region[;
 - said gate electrode being comprised of P-type polysilicon].
3. (Amended) The MOS gated device of claim 2 wherein said gate [dielectric] oxide has a thickness of between 500 to less than 1000Å.